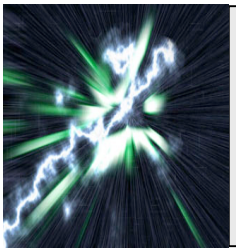

Call for Participation
Workshop on Silicon Errors in Logic – System Effects (SELSE 2010)

Stanford University— March 23-24, 2010

The growing complexity and shrinking geometries of modern device technologies are making high-density, low-voltage devices increasingly susceptible to influences from electrical noise, process variation, and natural radiation interference. System-level effects of these errors can be far reaching. Growing concern about intermittent errors, unstable storage cells, and the effects of aging are influencing system design. This workshop provides a forum for discussing current research and practice in system-level error management. Participants from industry and academia explore both current technologies and future research direction (including nanotechnology). We are interested in soliciting papers that cover system-level effects of errors from a variety of perspectives: architectural, logical and circuit-level, and semiconductor processes. Case studies are also solicited.

Key areas of interest are (but not limited to):

- Technology trends and the impact on error rates.
- New error mitigation techniques.
- Characterizing the overhead and design complexity of error mitigation techniques.
- Case studies describing the engineering tradeoffs necessary to decide what mitigation technique to apply.
- Experimental data.
- System-level models: derating factors and validation of error models.
- Error handling protocols (higher-level protocols for robust system design).

Authors may submit extended abstracts for paper presentation, poster presentation, or either format. The extended abstracts for accepted posters are included in the workshop proceedings. Authors are requested to submit their extended abstracts for review **before December 19, 2009**. Additional information and guidelines for submission are available at www.selse.org. Submissions should be PDF or Microsoft Word files that do not exceed four printed pages. Customary terms for copyright agreement and non-confidentiality will apply. Authors will be notified of paper outcome by February 10, 2010. Camera-ready formatted papers, up to six pages in length, are due on March 10, 2010.

Organizing committee (see www.selse.org/committee for complete membership):

Workshop Co-chairs:	Alan Wood, Sun
	Ishwar Parulkar
Program Co-chairs:	Allan Silburt and Adrian Evans, Cisco
	Charles Reccia, Intel
Finance Co-chairs	Vikas Chandra, ARM
	Rakesh Kumar, UIUC
Local Arrangements Chair:	Subashish Mitra, Stanford
Publicity Chair:	Vivian Zhu, TI